



January 1995  
Revised February 2005

## 74ABT126 Quad Buffer with 3-STATE Outputs

### General Description

The ABT126 contains four independent non-inverting buffers with 3-STATE outputs.

### Features

- Non-inverting buffers
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Disable time less than enable time to avoid bus contention

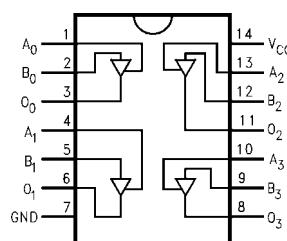
### Ordering Code:

Order Number	Package Number	Package Description
74ABT126CSC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ABT126CSJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT126CMTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ABT126CMTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.  
Pb-Free package per JEDEC J-STD-020B.

Note 1: "NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

### Connection Diagram



### Pin Descriptions

Pin Names	Descriptions
A <sub>n</sub> , B <sub>n</sub>	Inputs
O <sub>n</sub>	Outputs

### Function Table

Inputs	Output
A <sub>n</sub>	B <sub>n</sub>
H	L
H	H
L	X

H = HIGH Voltage Level  
L = LOW Voltage Level  
Z = HIGH Impedance  
X = Immaterial

Absolute Maximum Ratings <sup>(Note 2)</sup>				Recommended Operating Conditions		
Storage Temperature	–65°C to +150°C					
Ambient Temperature under Bias	–55°C to +125°C			Free Air Ambient Temperature	–40°C to +85°C	
Junction Temperature under Bias	–55°C to +150°C			Supply Voltage	+4.5V to +5.5V	
$V_{CC}$ Pin Potential to Ground Pin	–0.5V to +7.0V			Minimum Input Edge Rate ( $\Delta V/\Delta t$ )		
Input Voltage (Note 3)	–0.5V to +7.0V			Data Input	50 mV/ns	
Input Current (Note 3)	–30 mA to +5.0 mA			Enable Input	100 mV/ns	
Voltage Applied to Any Output in the Disabled or Power-Off State	–0.5V to 5.5V					
in the HIGH State	–0.5V to $V_{CC}$					
Current Applied to Output in LOW State (Max)	twice the rated $I_{OL}$ (mA)			<b>Note 2:</b> Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.		
DC Latchup Source Current (Across Comm Operating Range)	–300 mA			<b>Note 3:</b> Either voltage limit or current limit is sufficient to protect inputs.		
Over Voltage Latchup (I/O)	10V					
DC Electrical Characteristics						
Symbol	Parameter	Min	Typ	Max	Units	$V_{CC}$
$V_{IH}$	Input HIGH Voltage	2.0			V	
$V_{IL}$	Input LOW Voltage		0.8		V	
$V_{CD}$	Input Clamp Diode Voltage			–1.2	V	Min $I_{IN} = –18$ mA
$V_{OH}$	Output HIGH Voltage	2.5			V	Min $I_{OH} = –3$ mA
		2.0			V	Min $I_{OH} = –32$ mA
$V_{OL}$	Output LOW Voltage		0.55		V	Min $I_{OL} = 64$ mA
$I_{IH}$	Input HIGH Current		1		$\mu A$	$V_{IN} = 2.7$ V (Note 4)
			1		$\mu A$	$V_{IN} = V_{CC}$
$I_{BVI}$	Input HIGH Current Breakdown Test		7		$\mu A$	$V_{IN} = 7.0$ V
$I_{IL}$	Input LOW Current		–1		$\mu A$	$V_{IN} = 0.5$ V (Note 4)
			–1		$\mu A$	$V_{IN} = 0.0$ V
$I_{ID}$	Input Leakage Test	4.75			V	0.0 $I_{ID} = 1.9$ $\mu A$ , All Other Pin Grounded
$I_{OZH}$	Output Leakage Current		10		$\mu A$	0 – 5.5V $V_{OUT} = 2.7$ V; $\overline{OE}_n = 2.0$ V
$I_{OZL}$	Output Leakage Current		–10		$\mu A$	0 – 5.5V $V_{OUT} = 0.5$ V; $\overline{OE}_n = 2.0$ V
$I_{OS}$	Output Short-Circuit Current	–100	–275		mA	$V_{OUT} = 0.0$ V
$I_{CEX}$	Output HIGH Leakage Current		50		$\mu A$	$V_{OUT} = V_{CC}$
$I_{ZZ}$	Bus Drainage Test		100		$\mu A$	0.0 $V_{OUT} = 5.5$ V; All Others GND
$I_{CCH}$	Power Supply Current		50		$\mu A$	Max All Outputs HIGH
$I_{CCL}$	Power Supply Current		15		mA	Max All Outputs LOW
$I_{CCZ}$	Power Supply Current		50		$\mu A$	Max $\overline{OE}_n = V_{CC}$ ; All Others at $V_{CC}$ or Ground
$I_{CCT}$	Additional $I_{CC}$ /Input Outputs Enabled Outputs 3-STATE Outputs 3-STATE		1.5		mA	$V_I = V_{CC} – 2.1$ V
			1.5		mA	Enable Input $V_I = V_{CC} – 2.1$ V
			50		$\mu A$	Data Input $V_I = V_{CC} – 2.1$ V All Others at $V_{CC}$ or Ground
$I_{CCD}$	Dynamic $I_{CC}$ No Load (Note 4)		0.1		$mA/$ MHz	Max Outputs Open $\overline{OE}_n = GND$ , (Note 5) One Bit Toggling, 50% Duty Cycle

**Note 4:** Guaranteed, but not tested.**Note 5:** For 8 bits toggling,  $I_{CCD} < 0.8$  mA/MHz.

## AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^\circ C$ $V_{CC} = +5V$ $C_L = 50 pF$			$T_A = -40^\circ C$ to $+85^\circ C$ $V_{CC} = 4.5V-5.5V$ $C_L = 50 pF$		Units
		Min	Typ	Max	Min	Max	
$t_{PLH}$	Propagation Delay Data to Outputs	1.0	4.4		1.0	4.4	ns
$t_{PHL}$		1.0	4.6		1.0	4.6	
$t_{PZH}$	Output Enable Time	1.0	6.5		1.0	6.5	ns
$t_{PZL}$		1.0	6.5		1.0	6.5	
$t_{PHZ}$	Output Disable Time	1.0	5.8		1.0	5.8	ns
$t_{PLZ}$		1.0	5.5		1.0	5.5	

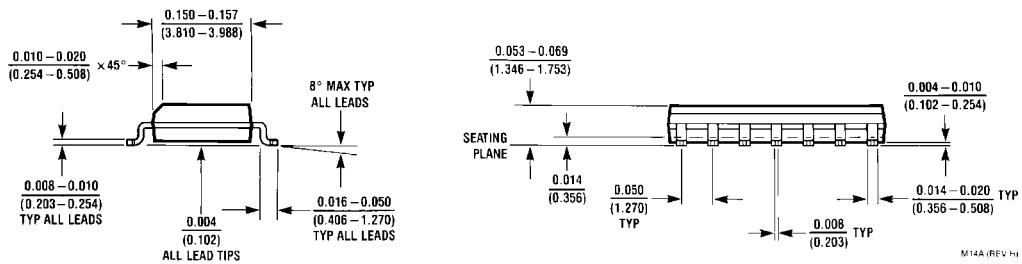
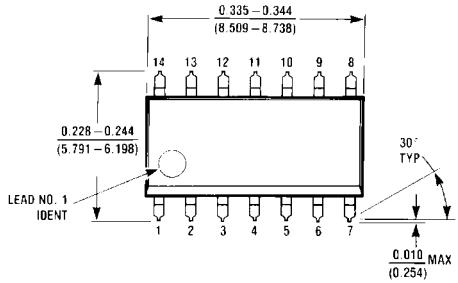
## Capacitance

Symbol	Parameter	Typ	Units	Conditions	
				$T_A = 25^\circ C$	
$C_{IN}$	Input Capacitance	5.0	pF	$V_{CC} = 0V$	
$C_{OUT}$ (Note 6)	Output Capacitance	9.0	pF	$V_{CC} = 5.0V$	

Note 6:  $C_{OUT}$  is measured at frequency  $f = 1$  MHz, per MIL-STD-883, Method 3012.

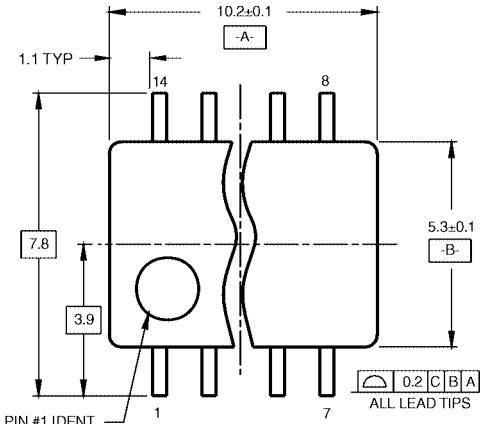
74ABT126

**Physical Dimensions** inches (millimeters) unless otherwise noted

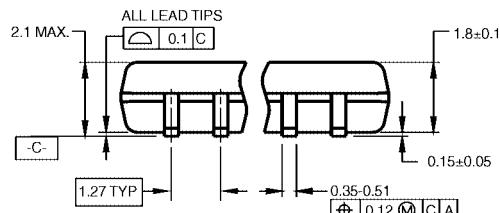


14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M14A

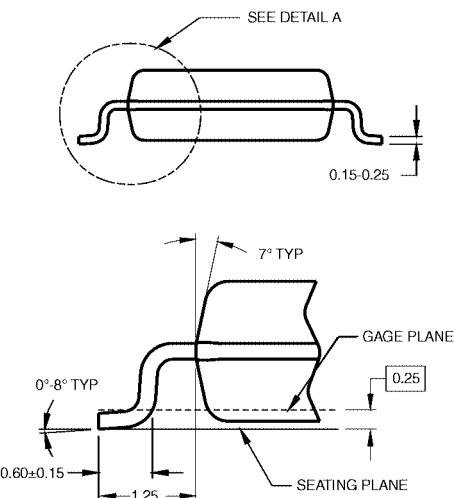
## **Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



#### LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

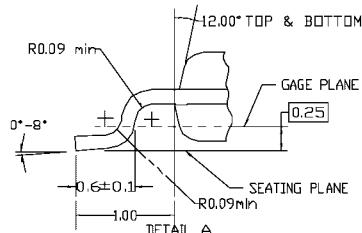
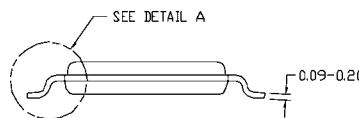
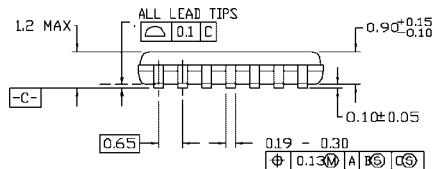
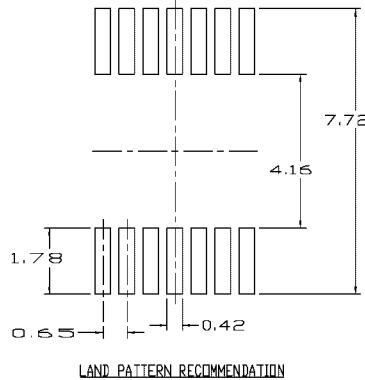
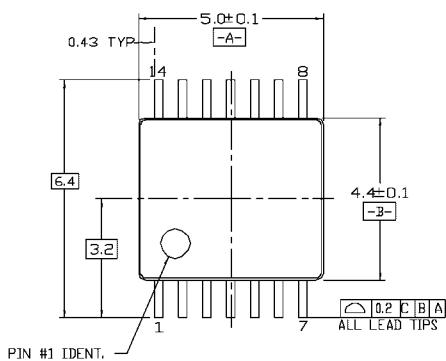
## NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

**Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M14D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC14

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)